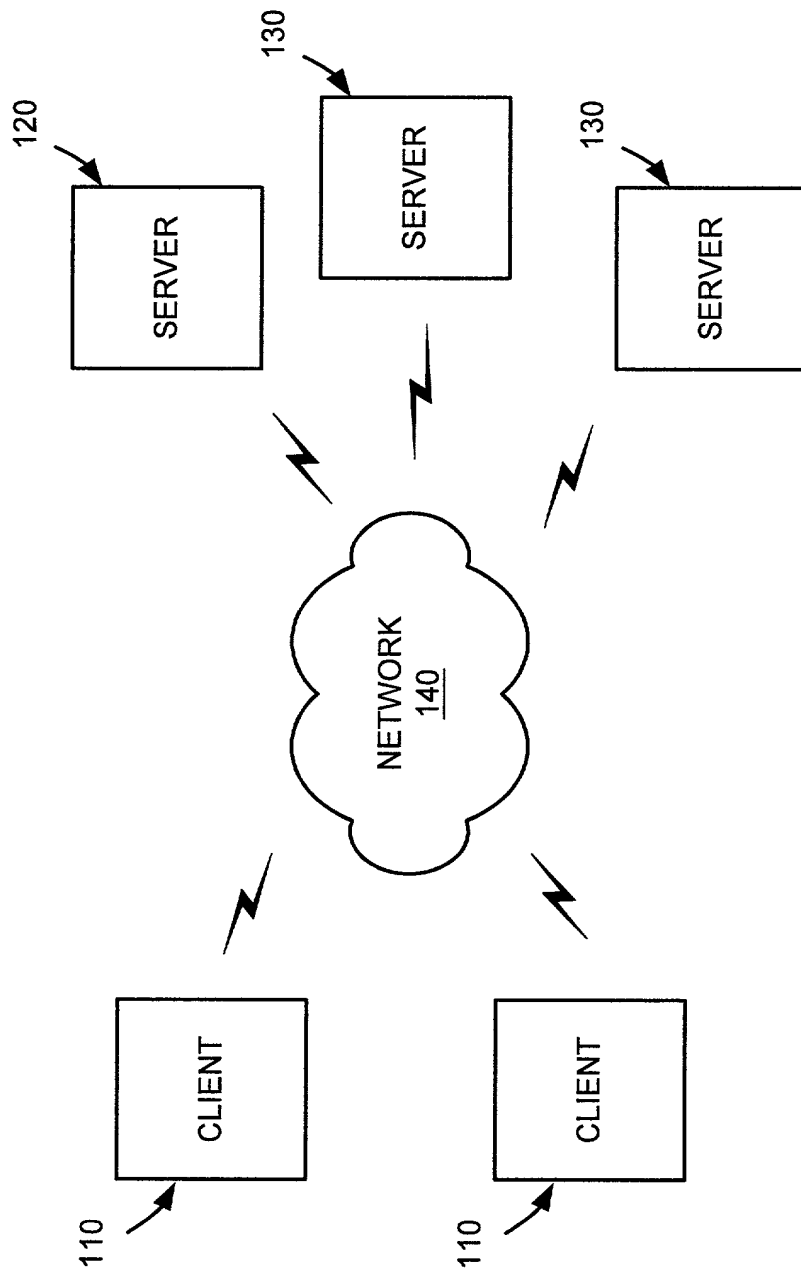
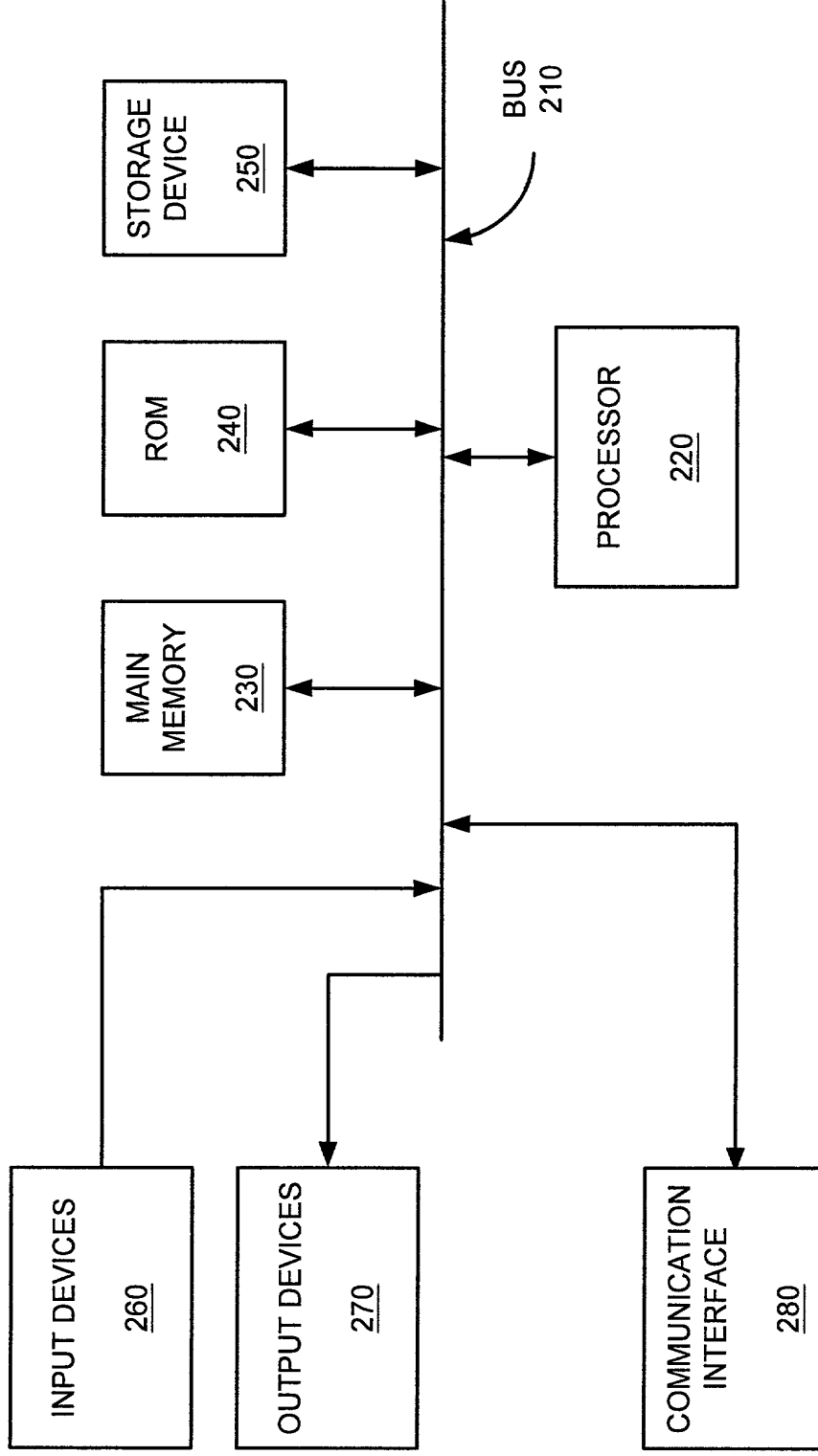


100 —→



**FIG. 1**

110 →



**FIG. 2**

230 →

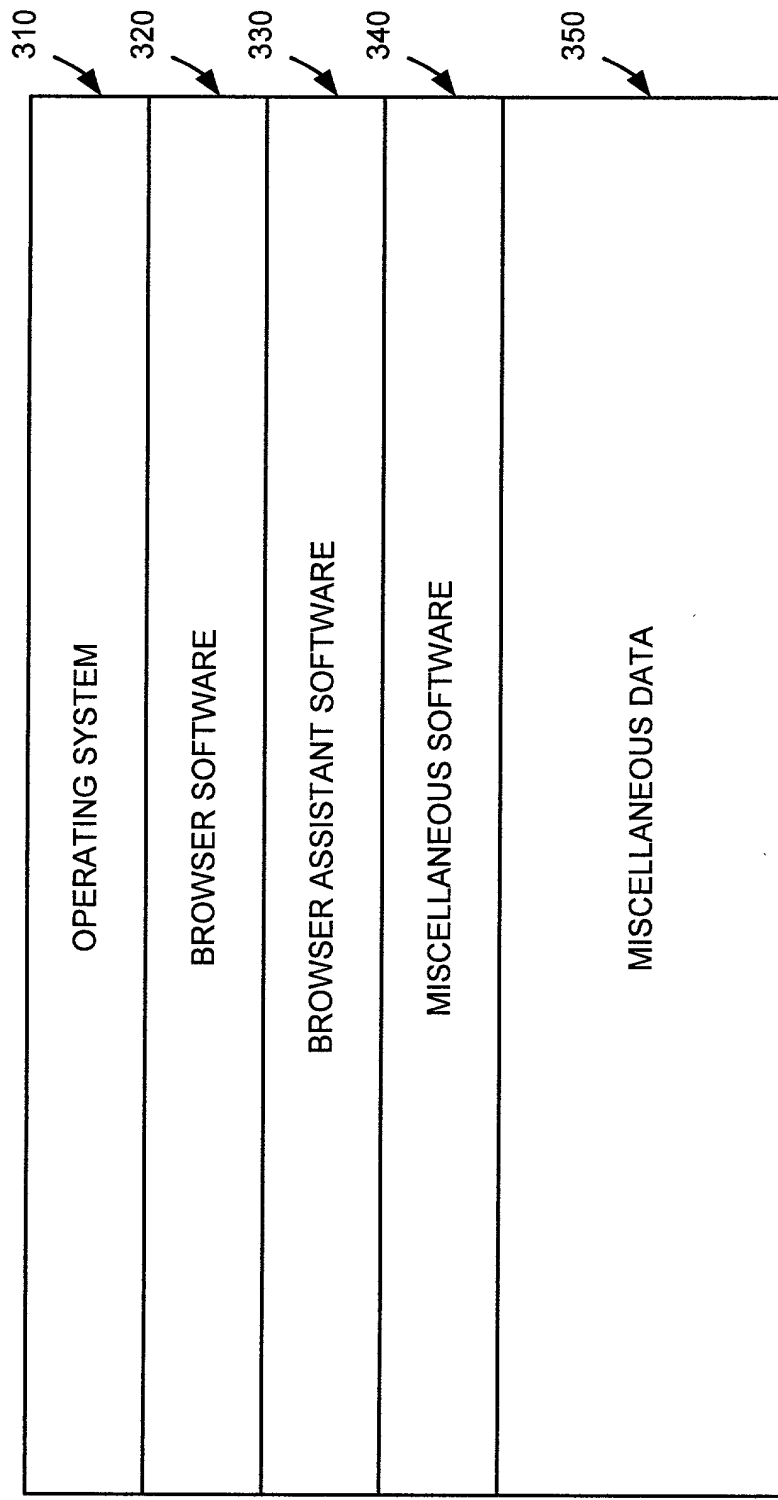


FIG. 3

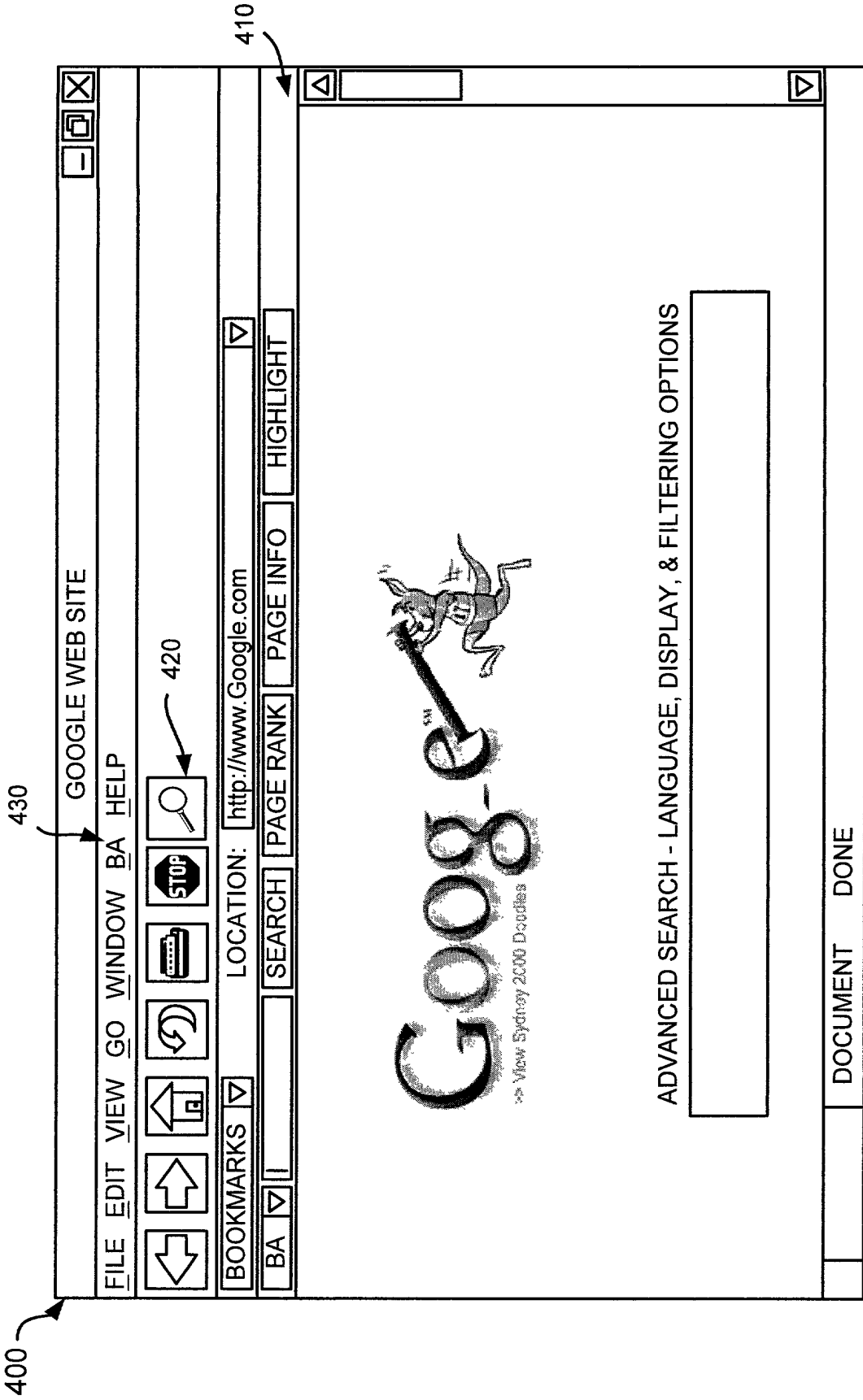


FIG. 4

FIG. 5 is a block diagram of a system 120. The system 120 includes a communication interface 560, a processor 520, memory 530, input devices 540, and output devices 550. The communication interface 560, processor 520, memory 530, input devices 540, and output devices 550 are connected to a bus 510. The bus 510 is a central line that allows data to be exchanged between the components. The communication interface 560 is connected to the bus 510 via a bidirectional arrow. The processor 520 is connected to the bus 510 via a bidirectional arrow. The memory 530 is connected to the bus 510 via a bidirectional arrow. The input devices 540 are connected to the bus 510 via a bidirectional arrow. The output devices 550 are connected to the bus 510 via a bidirectional arrow.

120 →

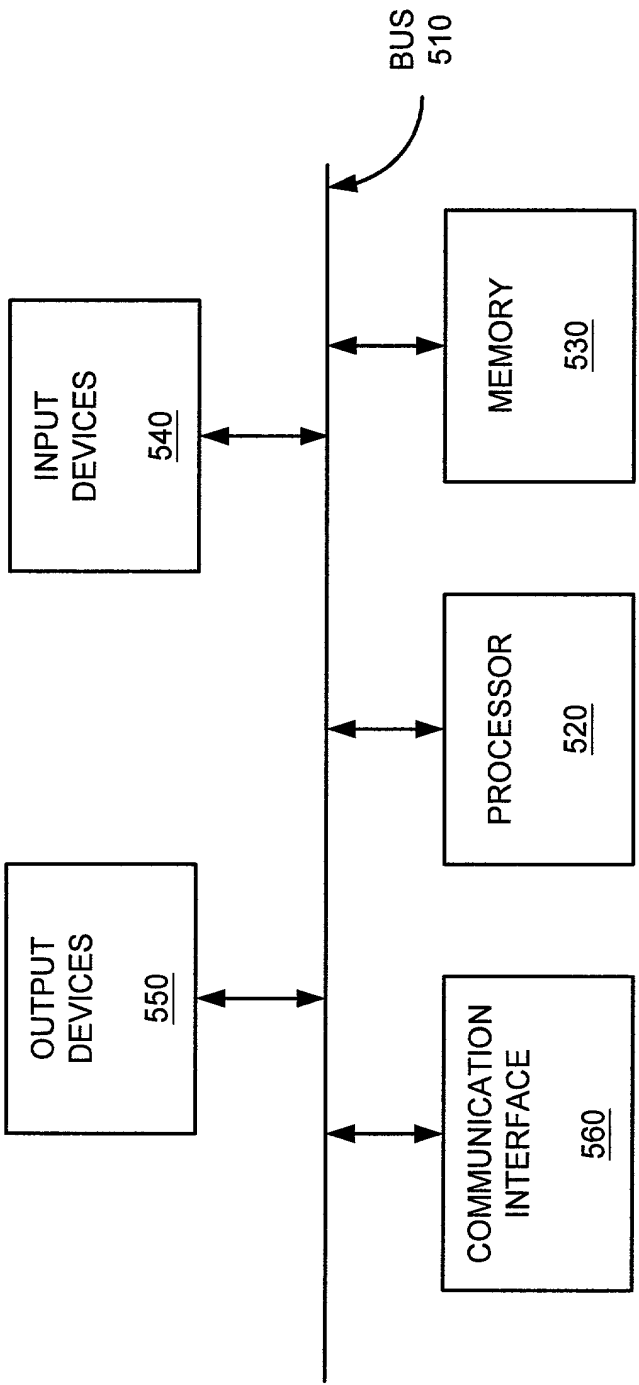
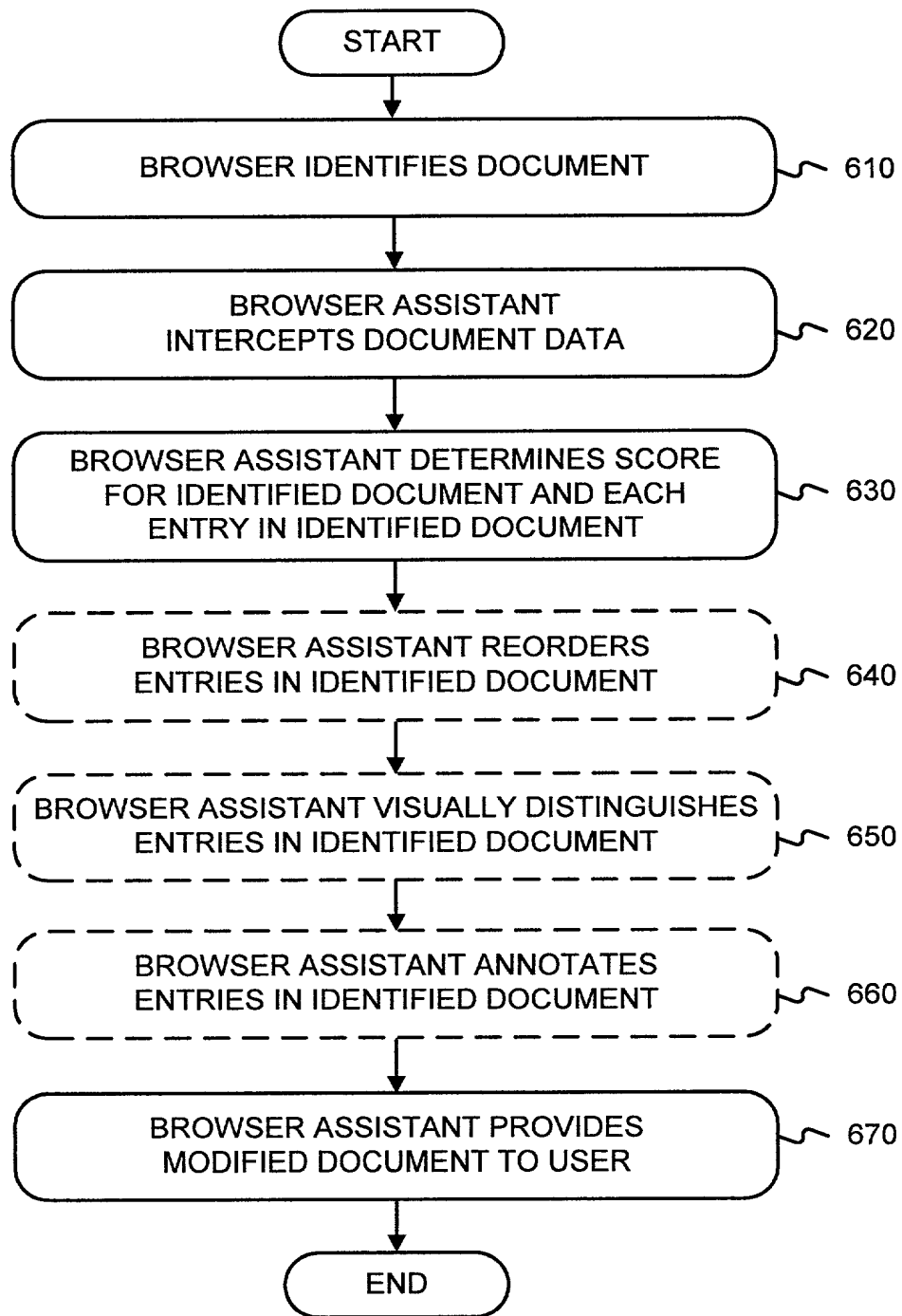


FIG. 5



**FIG. 6**

700 →

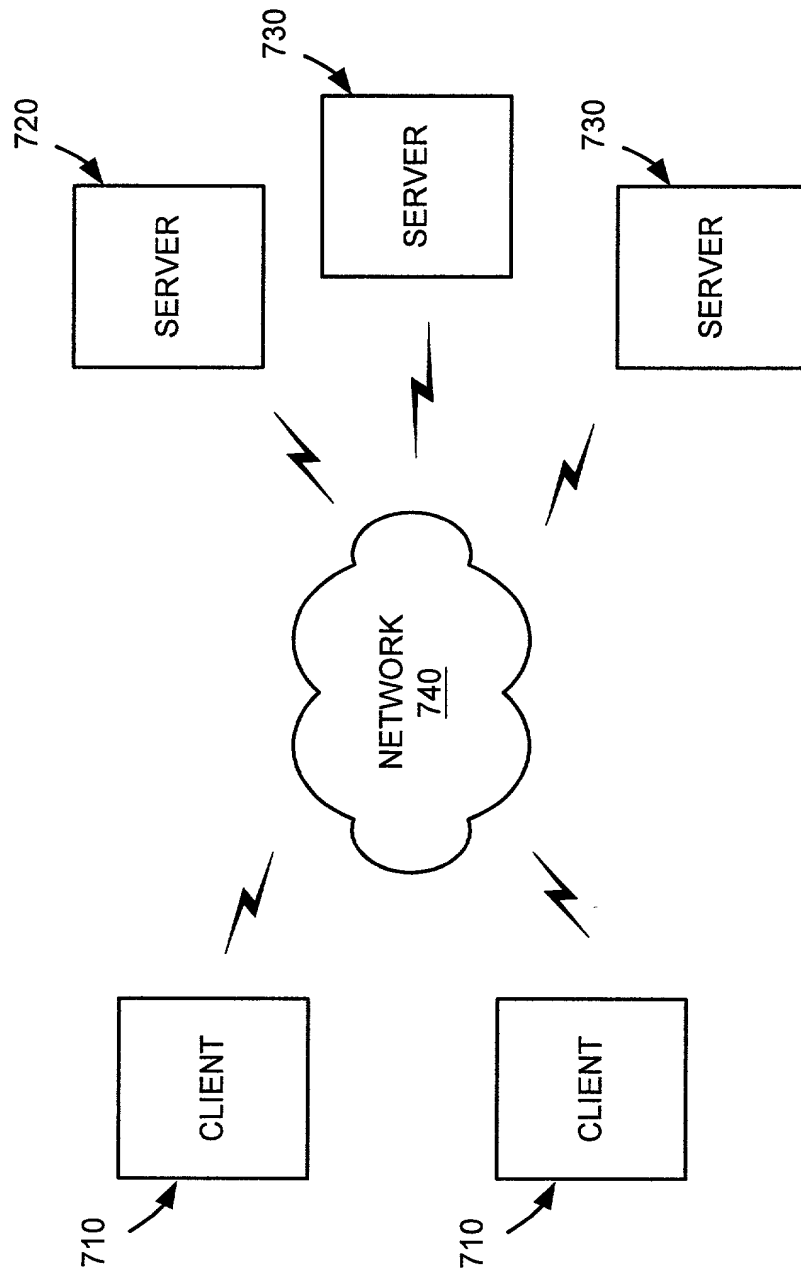
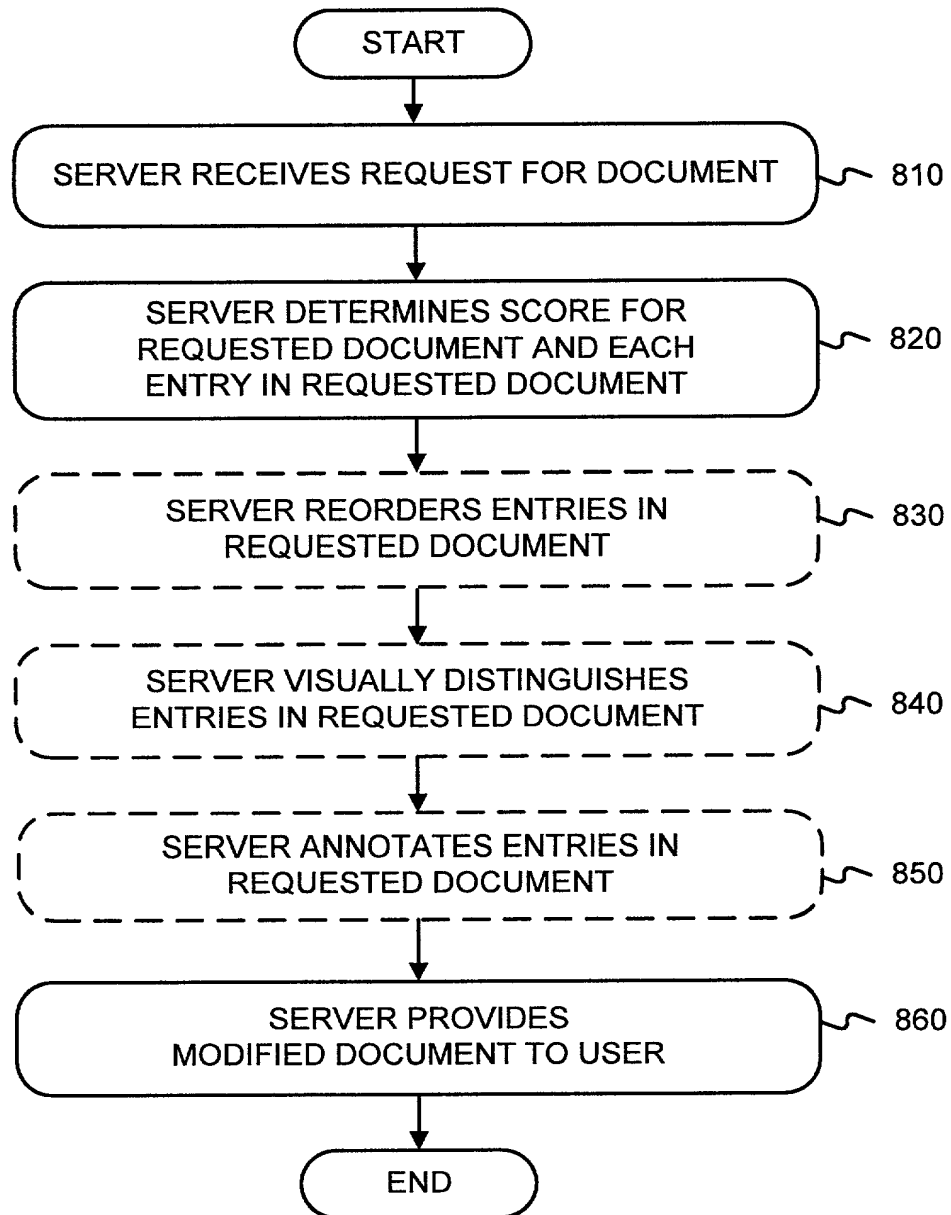


FIG. 7



**FIG. 8**